Theory of High Field Transport in Graphene Transistor

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Abstract

Negative Differential Resistance (NDR) behaviour is demonstrated in the output characteristics ($I_{ds}$-$V_{ds}$) of mono layer graphene transistor, under back gate condition. The transistor dimension (width and length) is shown to play an important role in the high field transport. Under certain design condition, the high field transport results in very good current saturation, instead of NDR. A device design guideline is provided to achieve one of these two conditions. Further the interplay between the channel charge injection in oxide, minority carrier injection at the drain and self heating through optical phonons determines the exact nature of high field transport have been demonstrated. Due to high power density, and lack of efficient heat removal through oxide, one can result in burn out of device due to thermal run away.

Keywords : phonon, negative differential resistence, SiO$_2$

1. Introduction

With the aggressive scaling of Silicon technology in the 22nm CMOS regime$^1$, several challenges have emerged in realizing further miniaturization of transistors. Both physical and technological limitations of silicon transistors, may force us to explore alternate materials technology to scale the transistors for sub-20nm dimensions. In this context, Graphene has shown a lot of promise as a potential alternate material to augment silicon transistors. Although Graphene has excellent transport properties$^2$, the lack of band gap has turned out be a serious limitation in
building reliable transistors. This limit is especially hurting in the digital CMOS applications. In any case, International Technology Roadmap for Semiconductors, has already included graphene as one of the potential vectors for device scaling. Table 1 illustrates the opportunities and challenges for graphene CMOS applications. Large scale deposition techniques, introducing controlled band gap, ability to deposit high-k dielectrics on graphene, realization of low resistivity contacts, achieving unipolar *n-channel* and *p-channel* transistors are still open challenges in the field. It appears that the analog CMOS applications are more imminent compared to digital CMOS.

**Table 1 :** Opportunities and challenges with graphene electronics

<table>
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<tr>
<th>Key Challenges</th>
<th>Target/Goal</th>
<th>Status</th>
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<tbody>
<tr>
<td>Ability to deposit Graphene with controlled thickness on Si compatible substrates</td>
<td>CVD?</td>
<td>No suitable integrated process available.</td>
</tr>
<tr>
<td>Ability to develop controlled badgap for high on-off ratio</td>
<td>Double gate architecture on SLG Confined lateral dimension on BLG</td>
<td>Control of bandgap still elusive.</td>
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<tr>
<td>High electron and hole mobility on Si compatible substrates</td>
<td>$\mu_n &gt; 20,000 \text{ cm}^2/\text{V}-\text{sec}$ $\mu_p &gt; 10,000 \text{ cm}^2/\text{V}-\text{sec}$</td>
<td>$\sim 8,000 \text{ cm}^2/\text{V-sec}$</td>
</tr>
<tr>
<td>Ability to deposit high-k gate dielectric</td>
<td>$D_{it} &lt; 10^{12}/\text{cm}^2\cdot\text{eV}$</td>
<td>Al$_2$O$_3$ has been tried, still needs optimization</td>
</tr>
<tr>
<td>Ability to depote n- and p-type</td>
<td>Co deposition of dopants, electron-hole puddle, ambipolar nature</td>
<td>Very sensitive to ambient condition</td>
</tr>
<tr>
<td>Ability to form low resistance contacts</td>
<td>Contact resistance less than $10^{-8} \Omega\cdot\text{cm}^2$</td>
<td>Needs more evaluation</td>
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However, for analog CMOS applications, especially in the very high frequency range, graphene transistors could still be very attractive. However, the high field transport and related device characteristics become very crucial for such applications. In this paper high field transport mechanisms in back gated single layer graphene transistors has been reported. Specifically authors demonstrate that the graphene transistor can either show a negative differential resistance or saturation characteristics, depending on the device dimensions. Authors further illustrate three important mechanisms, namely (i) channel carrier injection into gate oxide, (ii) drain side minority carrier injection and (iii) self heating through optical phonon coupling play a key role in dictating the high field transport.

2. Results and Discussion

The graphene transistors were created on a starting wafer with 300nm SiO$_2$ on highly doped n-type Silicon. The wafers were backed to remove any moisture and graphene was mechanically exfoliated. The single layer graphene regions were identified using Raman spectroscopy (Fig. 1). These locations were used for further processing of source/drain contacts. Electron beam lithography was used to define contact regions, and 50nm thick gold source/drain contacts were defined using lift off process. The back gate contact was realized by depositing 200nm Aluminum on the backside of the wafer. The device structure is schematically illustrated in Fig. 2. The SEM micrograph of the fabricated device is shown in Fig. 3. Several devices were fabricated with different channellength and width. The current-voltage (I-V) characteristics were measured using Agilent Semiconductor Device Analyzer. Fig. 4 demonstrates a well behaved back gated graphene transistor I-V characteristics. The Dirac point is close to 0V. The model predicted data, matches well with the experimental data. The current in the hole branch (negative Vg) is higher than the electron branch (positive Vg). This is because the gold contact is known to
dope graphene p-type, and hence the contact resistance is lower when the channel is hole doped (negative $V_g$), as against electron doped channel (positive $V_g$).

Fig. 1 Raman characterization to illustrate single layer exfoliated graphene

Fig. 2 Illustration of cross section of the fabricated transistor
In order to investigate the high field transport behaviour, the transistor was biased under large negative voltage, to heavily dope the channel with holes and then the source to drain voltage was varied to monitor the drain current. Bidirectional I-V sweeps were
also recorded to evaluate the presence of hysteresis in the I-V behaviour. Fig. 5 illustrates the typical I-V behaviour for 5 different transistors. Typically all transistors with width less than 15 micron exhibited negative differential resistance (NDR). As indicated in Fig. 5 the NDR regime, namely the decrease in drain current with increasing source-drain voltage, lasts over a very narrow range of source-drain bias voltages. After that the current starts increasing again, with increasing drain voltage. As shown in the inset of Fig. 5, we observe hysteresis in I-V characteristics. In particular, at a given bias voltage, the drain current value is higher during the forward sweep and it is much lower during reverse sweep. This is due to combination of two physical mechanisms. On one hand the holes attain sufficiently large energy under high fields, and these “hot holes” can be injected into the gate oxide, which reduces the gating efficiency during reverse sweep. In addition, the hot optical phonons generated under high fields reduce the carrier mobility during the reverse sweep, resulting in lower current. Authors further note that the current eventually turns around at larger voltages and increases with source-

Fig. 5 – Drain current versus source-drain voltage characteristics for 5 devices, illustrating negative differential resistance. The inset shows the hysteresis in bidirectional I-V sweep
drain voltage. This is due to the fact that under high drain electric fields, electrons can easily tunnel from the drain electrode into the channel due to the zero bandgap of graphene. Fig. 6 shows that the NDR is also evident in Ids-Vg characteristics, if the source-drain bias is set at large values, as seen in the hole branch of the Ids-Vg curve.

![Fig. 6 Negative differential resistance is also evident from Ids-Vg plot. When source-drain bias is set to a large value (5.5V) to cause self heating and carrier injection.](image)

Fig. 7 shows Ids-Vds characteristics for 3 devices with wider channel widths (26.1 μm, 28 μm, 29.6 μm). We notice that the NDR is absent from these devices, and in fact they show fairly good drain current saturation at high source-drain voltage. We explain this based on the gate electrostatic field controlling the drain injection. Fig. 8 demonstrates that the current saturation is seen only in wider transistors, whereas NDR is seen in narrow width transistors. The inset also shows the electric field lines for narrow and wide width devices. We see that in the narrow width devices, the back gate coupling on the channel is stronger and hence it does not allow drain injection to occur until drain voltage reaches very large values. Much before this NDR effect sets in and
hence we notice NDR in all the narrow width devices. On the other hand the gate coupling on the channel in wide width devises is not as strong and hence the drain injection sets in at about the same bias as the NDR sets in. Hence these to effect cancel out each other to a great extent, and hence the NDR is absent and we see current saturation behaviour.

Fig. 7 – Drain current versus source-drain voltage characteristics for 3 devices, illustrating current saturation behaviour.

Fig. 8 – The transistor design space (W and L space) to achieve either NDR (blue circles) or current saturation (green circles)
Based on all these experimental observations, the high field transport behaviour in graphene transistor can be explained based on the model illustrated in Fig. 9. At low drain voltages (region A) there is almost no self heating and also the channel carries do not have sufficient energy to get injected into the gate oxide. We see a linear Isd-Vds behaviour in this region. Subsequently, at higher drain voltages (region B), the hot optical phonons are generated due to self heating and this raises the temperature significantly. The carrier mobility will be degraded in this regime. In fact the fast

![Diagram of transport mechanism](image)

*Fig. 9 – The transport mechanism (A) low field linear region (B) onset of NDR due to optical phonons (C) plateauing of current due to onset of minority carrier injection at drain (D) drain injection taking over NDR effect*

current transient measurements\(^3\), reported by us elsewhere, clearly indicate that self heating can occur and reduce the current, even in the absence of carrier trapping in the gate oxide. However, during the DC measurements (illustrated in this work), the hot carriers in the channel can also gain sufficient energy to cross the graphene-oxide potential barrier, and get injected and trapped in the oxide. This will also contribute to the reduction in current in this region. In region C we see plateauing effect of current since the minority
carrier (electrons in this case) injection from drain starts becoming significant. Finally in region D, the drain injection takes over the NDR effect, and we see the increase in drain current with increase in drain voltage. Fig. 10 shows that the experimentally measured I-V characteristics can be matched fairly well with the model predicted characteristics, if we account for all the underlying mechanisms. In fact we further note that the transient measurements can be explaining by considering only self heating and drain injection, since the time constants associated with charge trapping (micro seconds) are much larger compared to measurement time (nano seconds). On the other hand the DC measurements (milli second to seconds) can be matched by taking into account all three mechanisms, namely i) channel carrier injection into gate oxide, ii) drain side minority carrier injection and iii) self heating through optical phonon coupling. We also note that the optical phonon temperature can be as high as 550 oK. In fact when the drain voltages are increased further, we see a destructive breakdown in the transistor resulting in open circuit and zero current. Failure analysis of such devices using SEM
analysis illustrates (Fig. 11) that the failure always occurs due to graphene breaking near the drain region, the hottest spot in the channel.

Fig. 11 Device burn out at drain junction due to thermal run-away

**Conclusion**

In summary authors have performed extensive analysis of high field transport in graphene, and demonstrated that NDR effect can be observed under certain conditions. In particular, narrow width devices, where minority carrier injection from the drain is delayed, NDR effect is always present due to self heating from hot optical phonons and hot carrier injection in the oxide. On the other hand wide transistors invariably show a fairly good drain current saturation. The results are explained based on the interplay between three physical mechanisms, namely i) channel carrier injection into gate oxide, ii) drain side minority carrier injection and iii) self heating through optical phonon coupling

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